

REMARKS

Applicants thank the Examiner for the courtesy of extending the October 6, 2010 telephone interview to Applicants' representative. As set forth below, Applicants have amended the claims along the lines set forth in the interview to expedite prosecution. The June 28, 2010 Final Office Action (Final Office Action) was based on pending Claims 3-7, 9-12 and 23-27. By this Amendment, Applicants amend Claims 3-7 and 9-12, cancel Claims 1, 2, 13-22 and 27 without prejudice or disclaimer, and add new Claims 28-36. Claim 8 was previously cancelled and Claims 23-26 remain as originally filed. Thus, after entry of this Amendment, Claims 3-7, 9-12 and 23-26 and 28-36 are pending and presented for further consideration.

REJECTION OF CLAIMS 3-7, 9-12 AND 23-27 UNDER 35 U.S.C. § 102(b)

The Office Action rejected Claims 3-7, 9-12 and 23-27 under 35 U.S.C. § 102(b) as being anticipated by Pilling. Applicants traverse the § 102(b) rejections of the claims, but have amended independent Claims 3-7 and 9-12 to expedite prosecution. The claims have been amended along the lines discussed in the interview in order to clarify the features of Applicants' inventions and expedite prosecution. Applicants additionally traverse the characterization of the pending claims, and each and every implicit and/or explicit official notice.

Claim 3

Amended Claim 3 recites:

a plurality of differential logic cells arranged in a combinatorial logic tree and each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, each of said plurality of differential logic cells configured to receive a precharge wave and/or a predischARGE wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said precharge wave and/or said predischARGE wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to

said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

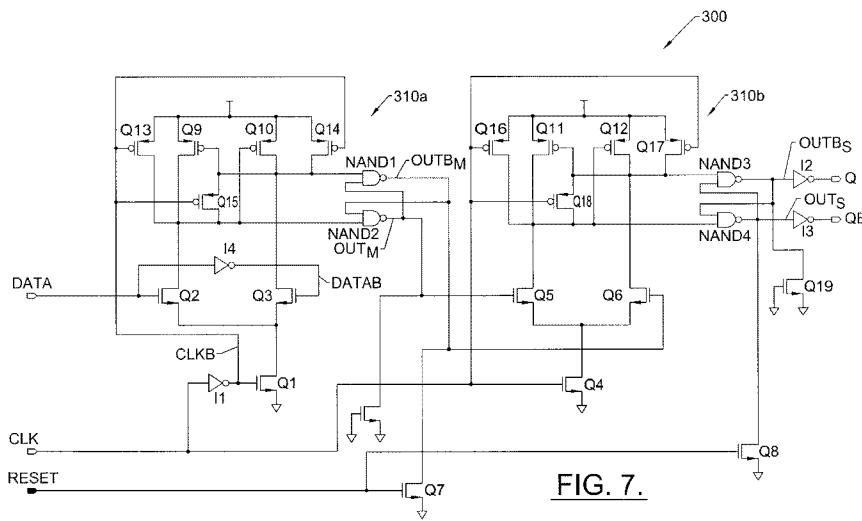
wherein each of said plurality of differential logic cells is configured to receive and propagate said precharge wave and/or said predischARGE wave during a precharge and/or pre-discharge phase, and is further configured to, during an evaluation phase, receive differential data on its inverted inputs and its corresponding non-inverted inputs and evaluate said differential data to produce differential output data on its inverted logic outputs and its non-inverted logic outputs,

wherein said precharge wave and/or said predischARGE wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of said plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is precharged or predischarged without distributing a separate precharge or predischARGE signal to the plurality of differential logic cells.

Amended Claim 3 is substantially different from Pilling. One advantage of certain embodiments of WDDL is that a pre-charge wave and/or a pre-discharge wave can be encoded in data received on the combinatorial data-bearing inputs and can be propagated from one WDDL differential logic cell to the next WDDL differential logic cell without distributing a separate pre-charge or predischARGE signal to the individual WDDL differential logic cells.

In contrast, Pilling is directed towards a flip-flop including a master stage and a slave stage. Pilling, Abstract. Figure 7 of Pilling, relied upon by the Office Action, is shown below.



The “CLK” signal of Pilling is not a “precharge wave and/or predischarge wave” within the meaning of Claim 3 and, to the extent that the “CLK” signal of Pilling may precharge or predischarge the Pilling circuit, the “CLK” signal must be distributed to each instance of the Pilling circuit. Moreover, the “CLK” signal is not received on a data bearing input of the Pilling circuit. Rather, the “CLK” signal does not represent a data value that alters the output value during an evaluation stage.

As such, among other things, Pilling does not teach or render obvious at least, **“wherein said precharge wave and/or said predischarge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of said plurality of differential logic cells.”**

Moreover, among other things, Pilling does not teach or render obvious at least **“wherein each of said plurality of differential logic cells is precharged or predischarged without distributing a separate precharge or predischarge signal to the plurality of differential logic cells.”**

For at least these reasons, Applicants respectfully submit that Claim 3 is patentably distinguished over Pilling.

Claim 4

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “said precharge wave and/or said predischARGE wave is encoded in data received on the inverting and non-inverting combinatorial data-bearing inputs of each of the plurality of differential logic cells, and wherein each of said plurality of differential logic cells is predischarged or precharged without distributing a separate predischARGE or precharge signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 4 is patentably distinguished over Pilling.

Claim 5

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and each of said plurality of differential logic cells is precharged without distributing a separate precharge signal to any of the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 5 is patentably distinguished over Pilling.

Claim 6

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “wherein said predischARGE wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and each of said plurality of differential logic cells is predischarged without distributing a separate predischARGE signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 6 is patentably distinguished over Pilling.

Claim 7

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “wherein said precharge wave is encoded in data received on the combinatorial data-bearing logic tree inputs of the first logic tree and the dual combinatorial data-bearing logic tree inputs of the second logic tree, wherein each of said first plurality of logic gates and each of said second plurality of logic gates is precharged or pre-discharged without distributing a separate precharge or pre-discharge signal to the first plurality of logic gates or to the second plurality of differential logic gates. ”

Moreover, Claim 7 is directed towards a **Divided** Wave Dynamic Differential Logic DPA-resistant logic circuit comprising “a single-ended first logic tree...produc[ing] first output data” and “a single-ended dual of said first logic tree...produc[ing] second output data,” where “the first output data comprises single-ended non-inverted output data and the second output data comprises corresponding single-ended inverted output data.” Figure 8 of the present application, shown below, illustrates an example embodiment of a Divided Wave Dynamic Differential Logic DPA-resistant logic circuit. One advantage of such a configuration is that the “single-ended dual logic tree” can be derived from the “single-ended first logic tree.” See, e.g., paragraphs 0063-0065.

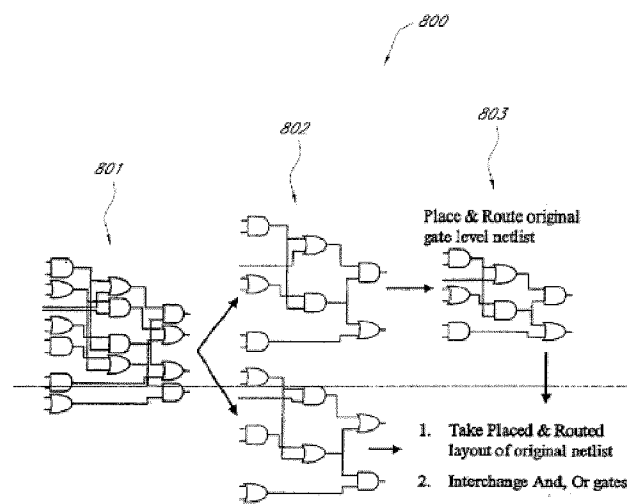


FIG. 8

In contrast, the cited portion of Pilling shows a master stage 310a that is in a serial configuration with a slave stage 310b. Moreover, both the master stage 310a and the slave stage 310b produce double-ended outputs, OUT_{B_M} , OUT_M and OUT_{B_S} , OUT_S , respectively, as shown in Figure 7 of Pilling. Thus, Pilling does not disclose or render obvious at least “**a first single-ended logic tree...**” and a “**a single-ended dual of said first single-ended logic tree connected in parallel with the first single-ended logic tree... the first output data comprising single-ended non-inverted output data and the second output data comprising single-ended corresponding inverted output data.**”

For at least these reasons, Applicants respectfully submit that Claim 7 is patentably distinguished over Pilling.

Claim 9

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and wherein each of said plurality of differential logic cells is pre-charged without distributing a separate pre-charge signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 9 is patentably distinguished over Pilling.

Claim 10

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and wherein each of said plurality of differential logic cells is pre-charged without distributing a separate pre-charge signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 10 is patentably distinguished over Pilling.

Claim 11

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “wherein said pre-discharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and wherein each of said plurality of differential logic cells is pre-discharged without distributing a separate pre-discharge signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 11 is patentably distinguished over Pilling.

Claim 12

For at least reasons similar to those discussed above with respect to Claim 3, Pilling does not teach or render obvious, among other things, “wherein said pre-discharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and wherein each of said plurality of differential logic cells is pre-discharged without distributing a separate pre-discharge signal to the plurality of differential logic cells.”

For at least these reasons, Applicants respectfully submit that Claim 12 is patentably distinguished over Pilling.

Dependent Claims 23-26

Dependent Claims 23-36 are believed to be patentable for the same reasons articulated above with respect to their respective independent claims. Dependent Claims 23-26 are also believed to be patentable because of the additional features recited therein.

Dependent Claim 27

Application No.: 10/586,846
Filing Date: July 20, 2006

As set forth above, dependent claim 27 has been cancelled without prejudice or disclaimer and the § 103 rejection of Claim 27 is therefore moot.

New Dependent Claims 28-36

New dependent Claims 28-36 have been added to further define Applicants inventions and are believed to be patentable for the same reasons articulated above with respect to their respective independent claims. Dependent Claims 28-36 are also believed to be patentable because of the additional features recited therein.

NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Applicants reserve the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution.

Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicants have made any disclaimers or disavowals of any subject matter supported by the present application.

OTHER APPLICATIONS OF ASSIGNEE

Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee:

Application No.: 10/586,846
Filing Date: July 20, 2006

Docket No.	Serial No.	Title	Filed
UCLARF.003DV1	12/191,144	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	August 13, 2008
UCLARF.003NP	10/565,551	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	September 11, 2006
UCLARF.008NP	12/092,687	Methods and Apparatus for Context-Sensitive Telemedicine	October 29, 2008
UCLARF.010A	12/167,062	Signal Decoder With General Purpose Calculation Engine	July 2, 2008

CONCLUSION / REQUEST FOR TELEPHONE INTERVIEW

In view of the foregoing amendments and remarks, Applicants respectfully request that the Examiner withdraw the outstanding rejections and allow the present application. If any issues arise during examination, the Examiner is invited to call the undersigned representative at his direct dial number listed below.

By focusing on specific claims and claim recitations in the discussion above, Applicants do not intend to imply that other claim recitations are disclosed or rendered obvious by the art of record.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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